REMARKS/ARGUMENTS

Claims 1-3, 7, 8, 12, 13 and 17-23 are pending in the present application. Claims 2, 3, 7, 8, 12 and 13 are withdrawn from consideration. Claims 4-6, 9-11 and 14-16 were previously cancelled and claim 20 is cancelled in this response. Claims 1, 17-19, and 21-23 are amended. Support for the claim amendments can be found in the specification on p.4, ll. 4-24; p. 10, l. 22 through p. 11, l. 6; p. 11, l. 26 through p. 15, l. 4; and Figures 3-7. No new matter is added. Reconsideration of the claims is respectfully requested.

I. 35 U.S.C. § 102, Asserted Anticipation – *Teodosiu*

The Examiner rejects claims 1, 17, 18, 20, 22, and 23 under 35 U.S.C. § 102(b) as anticipated by *Teodosiu*, Hive: Fault Containment for Shared-Memory Multiprocessors, SOSP '95 (hereinafter "*Teodosiu*"). This rejection is respectfully traversed.

> The examiner states that:
>
> **As per claims 1, 17, 18, 20, 22, and 23**, Teodosiu a teaches data processing system with programmable addressing, comprising:
> multifunctional input/output devices (cells) in a logical partition environment (Abstract, Teodosiu teaches a protection domain partition environment for distributed system of kernels called cells, wherein the cells comprises a network of nodes. Each node includes a processor and a memory that is a portion of the shared main memory.)
> control bits located in a memory, wherein the control bits allocate the multifunctional input/output devices into memory;
> an address bus leading the control bits to locations for the multifunctional input/output devices; and
> a programmable address control, wherein the programmable address control relocates individual functions. (See entire document, Figs. 3.1, 3.2, 3.3, 2.1)
> Teodosiu teaches isolating the processors and the processor's memory and of each cell from the remaining processors of the network in an arrangement wherein a memory coupled to processors is partitioned to isolate user applications from one another (WAX) by having each user application of the single CPU/memory system serviced by its own respective operating system within a partition. When the system boots, each cell is assigned a range of nodes that it owns throughout execution and each cell controls (inherently via control bits (data)) an allocated portion of the shared address space and runs as an independent multiprocessor kernel (respective operating system).

Office Action dated November 27, 2006, pp. 2-3.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed

invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). In this case each and every feature of the presently claimed invention is not identically shown in the cited reference, arranged as they are in the claims.

Amended claim 1 is as follows:

> 1. (Currently Amended) A data processing system with programmable addressing, comprising:
>
> at least one multifunctional input/output device operating in a logical partition environment, wherein the logical partition environment comprises a first operating system and a second operating system distinct from the first operating system;
>
> a memory coupled to the at least one multifunctional input/output device, wherein the memory contains a first set of control bits, wherein the first set of control bits allocate a first function of the multifunctional input/output devices into a first memory location of the memory, and wherein the first function is assigned to the first operating system;
>
> an address bus coupled to the at least one multifunctional input/output device, wherein the address bus allows transmission of the control bits between the at least one multifunctional input/output device and the memory; and
>
> a programmable address control coupled to the address bus, wherein the programmable address control relocates the first set of control bits from the first memory location to a second memory location in the memory, and wherein the second memory location is inaccessible to the first operating system.

The Examiner errs in asserting that *Teodosiu* anticipates original claim 1. *Teodosiu* does not teach multifunctional input/output devices **in a logical partition environment**, as recited in original claim 1 and as recited in currently amended claim 1.

Contrary to claim 1, *Teodosiu* teaches an operating system called Hive, with a kernel architecture that is structured as an internal distributed system of independent kernels called *cells* (Abstract). Each cell controls a portion of the global physical address space and runs as an independent multiprocessor *kernel* (Figure 3.1). However, *Teodosiu* does not teach a logical partition environment, as is required by claim 1.

Claim 1 as amended also requires that the logical partition environment comprise a first operating system and a second operating system. *Teodosiu* teaches only one operating system (Hive) running on a data processing system. Hive's kernel is partitioned into independent cells running independent kernels. However, running multiple independent kernels in a single operating system is not equivalent to running multiple operating systems on a single data processing system. In other words, a kernel is not the same as an operating system. (For further information, the examiner is invited to review the article found at

wiki.answers.com/Q/What_is_the_difference_between_a_Kernel_and_an_operating_system, which states, "An operating system, also known as an OS, is the software that makes a computer usable. The kernel is merely the 'core' or lowest level of an operating system.") Hence, a kernel is not an operating system. Therefore, *Teodosiu* does not teach "multifunctional input/output devices in a logical partition environment," as recited in claim 1.

Additionally, *Teodosiu* does not teach other features of amended claim 1. For example, *Teodosiu* does not teach the feature of, "a programmable address control coupled to the address bus, wherein the programmable address control relocates the first set of control bits from the first memory location to a second memory location in the memory, and wherein the second memory location is inaccessible to the first operating system." Thus, again, *Teodosiu* does not anticipate amended claim 1.

Because *Teodosiu* does not teach the features of amended claim 1, *Teodosiu* does not anticipate claim 1. Because claims 17, 18, 22, and 23 depend from claim 1, *Teodosiu* does not anticipate these claims at least by virtue of their dependency. Furthermore, claims 17, 18, 22, and 23 recite features not taught by *Teodosiu*. For example, *Teodosiu* does not teach the feature of, "wherein the inverter is programmable and may be changed based on any operating system environment and frequency of initialization," as in claim 22. Therefore, *Teodosiu* does not anticipate any of the currently pending claims. Accordingly, this rejection has been overcome.

II. 35 U.S.C. § 102, Asserted Anticipation – *Bouchier*

The Examiner rejects claims 1, 17, 18, 20, 22, and 23 under 35 U.S.C. § 102(e) as anticipated by *Bouchier, et al.*, Managing operations of a computer system having a plurality of partitions, U.S. Patent 6,684,343, January 27, 2004, (hereinafter "*Bouchier*"). Claim 20 has been canceled, thereby rendering moot the rejection with respect to claim 20. This rejection is respectfully traversed with respect to the remaining claims.

The examiner states that:

> **As per claims, 1, 17, 18, 20, 22, and 23**, Bouchier teaches a data processing system with programmable addressing, comprising:
> multifunctional input/output devices in a logical partition environment;
> control bits located in a memory, wherein the control bits allocate the multifunctional input/output devices into memory;
> an address bus leading the control bits to locations for the multifunctional input/output devices; and
> a programmable address control, wherein the programmable address control relocates individual functions. (col. 1, lines 58-cot. 13)
> Bouchier teaches a logical partition system environment having a group of cabinets wherein each cabinet contains a cell board. The cell board has a plurality of system CPUs/OS together with system memory with an I/0 connection controller (PCI, etc.). Each partition must have at least enough I/0

> attached to its cell board(s) to be able to boot the OS and each cell has a partition to communicate with one another and software or firmware running on a partition can operate the I/0 controllers to transfer data between system memory and external disks, networks, and multifunctional I/0 devices. The multiple copies of the OS are run independently of each other and control bits are utilized for allocation for each instance of the OS. Further, each partition that has its own cell boards with processors and memory and connected I/0 are isolated between different applications.

Office Action dated November 27, 2006, p. 4.

The Examiner errs in asserting that *Bouchier* anticipates original claim 1. For example, *Bouchier* does not teach a programmable address control, as recited in original claim 1. Additionally, *Bouchier* does not teach the newly claimed feature of, "a programmable address control coupled to the address bus, wherein the programmable address control relocates the first set of control bits from the first memory location to a second memory location in the memory, and wherein the second memory location is inaccessible to the first operating system," as in amended claim 1. Instead, *Bouchier* only teaches a service processor capable of monitoring and controlling the operation of the multiple partitions and the hardware assigned to them. The service processor also performs operational and diagnostic and debugging functions (col. 1, lines 47-53; col. 2, lines 27-28). However, *Bouchier* does not teach the features described above.

Because claims 17, 18, 22, and 23 depend from claim 1, *Bouchier* does not anticipate these claims at least by virtue of their dependency. Furthermore, claims 17, 18, 22, and 23 recite features not anticipated by *Bouchier*. For example, *Bouchier* does not teach the feature of, "wherein the inverter is programmable and may be changed based on any operating system environment and frequency of initialization," as in claim 22. Therefore, *Bouchier* does not anticipate any of the currently pending claims. Accordingly, this rejection has been overcome.

III. 35 U.S.C. § 103, Obviousness

The Examiner rejects claims 19 and 21 under 35 U.S.C. § 103 as obvious over *Teodosiu* or *Bouchier* in view of *Nale*, Configurable Address Line Inverter For Remapping Memory, U.S. Patent 5,987,581, November 16, 1999, (hereinafter "*Nale*"). This rejection is respectfully traversed.

The examiner states that:

> **As per claims 19 and 21**, Hive and Bouchier both disclose a method of a programmable address control for resource reallocation of services for multifunctional devices and protecting/isolating partitions running multiple instances of operating systems, however, Hive nor Bouchier specifically teach inserting an inverter on an address bus for the multifunctional input/output device. Nonetheless, Nale teaches selectively inverting the state of an address line on an address bus that includes a selectable inverter element and a control

> circuit. This method taught by Nale prevents two blocks from accessing the same location in the system memory. (Nale, cols.1-9) Therefore, it would have been obvious to one of ordinary skill at the time the invention was made to implement the method of inverting the state of an address line on an address bus into Hive and Bouchier partition environment system because doing to would add and expand the flexibility of both systems and further enhance the protection/isolation of partitions by preventing certain partitions from accessing similar memory locations.

Office Action dated November 27, 2006, pp. 5-6.

III.A. No *Prima Facie* Case of Obviousness Can Be Stated Because the References Do Not Teach or Suggest All the Features of Amended Claim 1

Regarding claims 19 and 21, no *prima facie* obviousness rejection can be made because the proposed combination does not teach or suggest all of the features of claims 19 and 21. A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). In the case at hand, not all of the features of the claimed invention have been properly considered and the teachings of the references themselves do not teach or suggest the claimed subject matter to a person of ordinary skill in the art.

No *prima facie* obviousness rejection can be made because neither *Teodosiu* nor *Bouchier* teach or suggest all features of claim 1, from which claim 17 and 19 depend. As shown above, *Teodosiu* does not teach the claimed feature of, "a programmable address control coupled to the address bus, wherein the programmable address control relocates the first set of control bits from the first memory location to a second memory location in the memory, and wherein the second memory location is inaccessible to the first operating system" as recited in amended claim 1. Furthermore, because *Teodosiu* is not directed to the claimed features in a logical partition environment, *Teodosiu* also does not suggest the features of amended claim 1.

Additionally, *Bouchier* also does not teach or suggest all of the features of amended claim 1. *Bouchier* teaches monitoring multiple partitions using a service processor. However, *Bouchier* does not teach "a programmable address control coupled to the address bus, wherein the programmable address control relocates the first set of control bits from the first memory location to a second memory location in the memory, and wherein the second memory location is inaccessible to the first operating system," as recited in amended claim 1. *Bouchier* states the following in regard to the functions provided by the service processor:

> The service processor provides many general supportability and manageability features such as a user interface to control and monitor the complex. Of particular relevance to the inventive system are the following functions performed by the service processor:
>
> Allow the user to physically connect to the service processor (e.g. RS232 connectors, LAN connectors).
>
> Allow the user to become logically connected to the service processor (e.g. log in).
>
> Provide a user interface (e.g. menus, ability to type commands) to the connected and logged in user, by which means the user can perform monitoring and control operations on the complex hardware, such as power on/off or display status or view logged events.
>
> Allow the receiving and logging of events and the reflection of the logged events to the partitions.
>
> Support the network connection to a JTAG scan diagnostic, and to a firmware update utility and to a debugger.

Bouchier, col. 5, line 56 – col. 6, line 7.

As stated above, the service processor provides many general supportability and manageability features such as a user interface to control and monitor the complex. The above portion of *Bouchier* discloses the functions performed by the service processor. Neither this portion nor any other portion of *Bouchier* teaches "a programmable address control coupled to the address bus, wherein the programmable address control relocates the first set of control bits from the first memory location to a second memory location in the memory, and wherein the second memory location is inaccessible to the first operating system," as recited in claim 1. Furthermore, because *Bouchier* specifically describes the functions performed by the service processor in the above cited paragraph without any reference to a programmable address control, as claimed, *Bouchier* also does not suggest the features of claim 1.

Furthermore, *Nale* does not teach or suggest "a programmable address control coupled to the address bus, wherein the programmable address control relocates the first set of control bits from the first memory location to a second memory location in the memory, and wherein the second memory location is inaccessible to the first operating system," as recited in claim 1. *Nale* provides a method of mapping an address to the ROM system space (col. 3, lines 23-25). *Nale* includes an apparatus for selectively inverting the state of an address line on an address bus (col. 2, lines 58-59). However, *Nale* does not teach a "a programmable address control coupled to the address bus, wherein the programmable address control *relocates the first set of control bits from the first memory location to a second memory location in the memory*, and wherein the second memory location is inaccessible to the first operating system," as recited in claim 1. Thus, *Nale* does not teach or suggest the features of amended claim 1.

Because none of *Teodosiu*, *Bouchier*, or *Nale* teach or suggest "a programmable address control coupled to the address bus, wherein the programmable address control relocates the first set of control bits from the first memory location to a second memory location in the memory, and wherein the second

memory location is inaccessible to the first operating system," as recited in amended claim 1, the proposed combination of the references when examined as a whole does not teach or suggest all of the features of amended claim 1. Accordingly, no *prima facie* obviousness rejection can be made against amended claim 1.

Neither *Teodosiu* nor *Bouchier* teach or suggest this claimed feature. Because *Nale* also does not teach or suggest this claimed feature, the proposed combination of these references, when considered as a whole, does not teach or suggest all of the features of claims 19 and 21. Therefore, no *prima facie* obviousness rejection can be stated against these claims.

III.B. No Need Exists to Combine the References

In addition, *Teodosiu* has no need for inverting the state of an address line on an address bus. The Examiner states that inverting the state of an address line on an address bus would further enhance the protection/isolation of partitions by preventing certain partitions from accessing similar memory locations. However, *Teodosiu* already teaches a method for preventing certain partitions from accessing similar memory locations. *Teodosiu* implements an OS with independent kernels called cells and each cell controls a portion of the physical address space and runs an independent multiprocessor kernel. Thus, *Teodosiu* has no need for inverting the state of an address line on an address bus.

Furthermore, *Bouchier* has no need for inverting the state of an address line on an address bus. *Bouchier* is directed towards a service processor for performing diagnostic functions and for monitoring partitions. *Bouchier* allows system control features such as power on/off, status display, etc. for multiple cabinets *under control* of the service processor (Abstract). Thus, *Bouchier* has no need for inverting the state of an address line on an address bus to prevent certain partitions from accessing similar memory locations, as the service processor already performs that function.

If no need for the combination exists, no pre-existing teaching, suggestion, or motivation to combine the references exists. Accordingly, no *prima facie* obviousness rejection can be stated against claims 19 and 21.

IV. Conclusion

The subject application is patentable over the cited references and should now be in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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